AMENDMENT TO THE CLAIMS

Please **CANCEL** claims 26-30.

A copy of all pending claims and a status of the claims is provided below.

Claim 1. (Original) A method of forming a semiconductor structure comprising steps of:

forming spacer voids between a gate a the mandrel layer;

creating recesses in a substrate below and in alignment with the spacer voids;

filling a first portion of recesses with a stress imposing material;

filling a second portion of the recesses with a semiconductor material; and

removing the mandrel layer.

Claim 2. (Original) A method according to claim 1, further including forming dummy spacers between the mandrel layer and the gate and forming a nitride interface as an etch stop in the recesses.

Claim 3. (Original) A method according to claim 1, wherein the recesses include a first recess and a second recess, the first recess and the second recess having a depth greater than a depth of the bottom of a channel area of the gate.

Claim 4. (Original) A method according to claim 3, wherein the first recess has a depth substantially equal to the depth of the second recess.

Claim 5. (Original) A method according to claim 3, wherein the first recess has a depth of about 500 to 2000 angstroms.

Claim 6. (Original) A method according to claim 1, further comprising forming dummy spacers and removing the dummy spacers to form the spacer voids, wherein:

a first dummy spacer has a first width;

a second dummy spacer has a second width;

a first recess of the recesses has a width substantially equal to the first width of the first dummy spacer; and

a second recess of the recesses has a width substantially equal to the second width of the second dummy spacer.

Claim 7. (Original) A method according to claim 6, wherein the first width is substantially equal to the second width.

Claim 8. (Original) A method according to claim 7, wherein the first width is about 100 to 1000 Å.

Claim 9. (Original) A method according to claim 1, wherein the recesses are substantially equidistant from the gate.

Claim 10. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a compressive stress.

Claim 11. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a tensile stress.

Claim 12. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a stress that degrades electron or hole mobility in the semiconductor structure.

Claim 13. (Original) A method according to claim 1, wherein the stress imposing material is a material that introduces a stress that enhances electron or hole mobility in the semiconductor structure.

Claim 14. (Original) A method according to claim 1, wherein the stress imposing material is a material comprised of at least one of polysilicon, SiO_2, $Si_{1-x}Ge_x$, Si_xN_y, or Si_xON_y.

Claim 15. (Original) A method according to claim 1, wherein the semiconductor material is comprised of epitaxially grown Si.

Claim 16. (Original) A method according to claim 1, wherein:

the gate is an n-channel field effect transistor gate; and

the stress imposing material is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate.

Claim 17. (Original) A method according to claim 1, wherein:

the gate is a p-channel field effect transistor gate; and

the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

Claim 18. (Original) A method according to claim 1, further comprising a step of annealing after filling the first portion of the first recess and the first portion of the second recess with a stress imposing material.

Claim 19. (Original) A method of forming a semiconductor structure comprising steps of:

forming first dummy spacers on sides of a gate formed on a substrate;

forming a mandrel layer with portions of the mandrel layer abutting the dummy spacers;

removing the dummy spacers to form spacer voids between the gate and mandrel layer;

creating recesses in the substrate below and in alignment with the spacer void;

filling a first portion of the recesses with a stress imposing material; and

filling a second portion of the recesses with a semiconductor material.

Claim 20. (Original) A method according to claim 19, further comprising the steps of:

filling a second portion of the recesses with a semiconductor material; and

removing the mandrel layer, wherein:

the first portion of the recesses is below the bottom of a channel area of the gate; and

the stress imposing material is a material that introduces one of a compressive stress and a tensile stress in the channel area.

Claim 21. (Original) A method according to claim 19, wherein the stress imposing material is a material comprised of at least one of polysilicon, SiO_2, $Si_{1-x}Ge_x$, Si_xN_y, or Si_xON_y.

Claim 22. (Original) A method according to claim 20, wherein the gate is one of:

an n-channel field effect transistor gate and the stress imposing material is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate; and

a p-channel field effect transistor gate and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

Claim 23. (Original) A method of forming a semiconductor structure comprising steps of:

forming a first type of field effect transistor gate and a second type of field effect transistor gate on a substrate;

forming a first dummy spacer and a second dummy spacer on sides of the first type of field effect transistor gate and on sides of the second type of field effect transistor gate;

forming a mandrel layer with first portions of the mandrel layer abutting the first and second dummy spacers for the first type of field effect transistor gate and second portions of the mandrel layer abutting the first and second dummy spacers for the second type of field effect transistor gate;

masking the second type of field effect transistor gate and the first and second dummy spacers for the second type of field effect transistor gate and introducing stress material for the first type of field effect transistor gate;

masking the first type of field effect transistor gate and the first and second dummy spacers for the first type of field effect transistor gate and introducing stress material for the first type of field effect transistor gate; and

removing the mandrel layer;

wherein the step of introducing stress material is comprised of

removing the first and second dummy spacers from the unmasked field effect transistor gate to form first and second spacer voids between the gate and first portions of the mandrel layer;

creating a first recess in the substrate below and in alignment with the first spacer void and a second recess in the substrate below and in alignment with the second spacer void for the unmasked field effect transistor gate;

filling a first portion of the first recess and a first portion of the second recess for the unmasked field effect transistor gate with a stress imposing material configured to enhance performance of the unmasked field effect transistor gate;

filling a second portion of the first recess and a second portion of the second recess for the unmasked field effect transistor gate with a semiconductor material; and

unmasking the masked field effect transistor gate and the first and second dummy spacers for the masked field effect transistor gate.

Claim 24. (Original) A method according to claim 23, wherein the steps are performed in the order recited.

Claim 25. (Original) A method according to claim 23, wherein:

the first type of field effect transistor gate is an n-channel field effect transistor gate and the stress imposing material configured to enhance performance of the n-channel field effect transistor gate is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate; and

the second type of field effect transistor gate is a p-channel field effect transistor gate and the stress imposing material configured to enhance performance of the p-channel field effect transistor gate is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate.

Claims 26-30. (cancel)